

LOK JAGRUTI UNIVERSITY (LJU)
INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer science & Design (703)

Bachelor of Technology (B.E.) – Semester - IV

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| Course Code: | 017033493 |
| Course Name: | Computer Organization & Architecture |
| Category of Course: | Professional Core Course (PCC) |
| Prerequisite Course: | Digital Electronics (017033391) |

| Teaching Scheme | | | | |
|-----------------|--------------|---------------|--------|-------------|
| Lecture (L) | Tutorial (T) | Practical (P) | Credit | Total Hours |
| 4 | 1 | 0 | 5 | 50 |

| Syllabus | | | | |
|---|---|--|--|----------------|
| Unit No. | Topic | Prerequisite Topic | Post requisite Topic | Teaching Hours |
| 01 | Data Representation | | | 2 (02%) |
| | 1.1 Fixed Point Representation | ---- | ---- | |
| | 1.2 Floating Point Representation | ---- | ---- | |
| 02 | Register Transfer and Micro-operations | | | 5 (10%) |
| | 2.1 Register Transfer Language | ---- | Microprocessor-8086 (017033501- Unit-2.1,2.2,2.3) | |
| | 2.2 Bus and Memory Transfers | Multiplexers, Decoders (017033391- Unit-6.1,6.2) | | |
| | 2.3 Arithmetic, Logic and Shift Micro-operations | Binary Arithmetic and logical operations (017033391- Unit-2.1, 2.2), Adders (017033391-Unit-5.2, 5.3, 5.4) | ---- | |
| 2.4 Arithmetic Logical Shift Unit | ---- | | | |
| 03 | Basic Computer Organization | | | 6 (12%) |
| | 3.1 Instruction Codes, Computer Registers | ---- | ---- | |
| | 3.2 Computer Instructions | ---- | ---- | |
| | 3.3 Instruction Cycle | | | |
| | 3.4 Timing and Control | Computer Registers (017033493 - Unit- 3.1), Computer Instructions (017033493 - Unit-3.2) | ---- | |
| 04 | Basic Computer Design | | | 4 (08%) |
| | 4.1 Memory and Register-Reference Instructions | ---- | ---- | |
| | 4.2 Input-Output Instructions | ---- | ---- | |
| | 4.3 Interrupt Cycle | | Microprocessor8086 (017033501-Unit-5.2) | |
| 05 | Programming the Basic Computer | | | 8 (18%) |
| | 5.1 Machine Language, Assembly Language | ---- | Microprocessor-8086 (017033501-Unit-3.1) | |
| | 5.2 Assembler, First Pass, Second Pass | Assembly Language (017033493 - Unit- 5.1) | ---- | |
| | 5.3 Program Loops | | ---- | |
| | 5.4 Subroutines | Assembly Language (017033493 - Unit- 5.1), Program Loops (017033493 - Unit- 5.3) | ---- | |
| 5.5 General Register Organization, Stack Organization | ---- | | | |
| 06 | Central Processing Unit | | | 8 (12%) |
| | 6.1 Instruction Formats, Addressing Modes | Computer Instructions (017033493 - Unit- 3.2) | ---- | |
| | 6.2 Data Transfer and Manipulations, Program Control | Computer Instructions (017033493 - Unit- 3.2) | ---- | |
| | 6.3 RISC Computer, CISC Computer | ---- | ---- | |
| 07 | Pipeline Processing | | | 5 (10%) |
| | 7.1 Parallel Processing, Flynn's classification, Pipelining | ---- | ---- | |
| | 7.2 Arithmetic Pipeline | Pipelining (017033493 - Unit-7.1) | ---- | |
| | 7.3 Instruction Pipeline | | ---- | |
| 7.4 RISC Pipeline | ---- | | | |
| 08 | Computer Arithmetic | | | 2 (05%) |
| | 8.1 Integer Numbers: Sign-Magnitude, 1's complement, 2's complement | Binary Arithmetic and logical operations (017033391- Unit-2.1, 2.2) | ---- | |
| 8.2 Addition and Subtraction | ---- | | | |
| 09 | Memory Organization | | | 6 (14%) |
| | 9.1 Multiplication Algorithms (Booth Multiplication Algorithm), Division Algorithms | ROM (017033391- Unit-9.1) | ---- | |
| | 9.2 Memory Hierarchy, Main Memory, Auxiliary Memory | ---- | ---- | |
| | 9.2 Associative Memory | ---- | ---- | |
| | 9.3 Cache Memory | ---- | ---- | |
| 10 | Input-Output Organization | | | 4 (09%) |
| | 10.1 Input-Output Interface, Asynchronous Data Transfer | ---- | ---- | |
| | 10.2 Memory Mapped I/O, I/O mapped I/O, Modes of Transfer, Priority Interrupt | ---- | ---- | |

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| 10.3 Direct Memory Access (DMA) | ----- | Microprocessor-8086 (017033501-Unit-8.1) |
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**Proposed Theory + Practical Evaluation Scheme by Academicians
(% Weightage Category Wise and it's Marks Distribution)**

L: 4 T: 1 P: 0

**Note: In Theory Group, Total 4 Test (T1+T2+T3+T4) will be conducted for each subject.
Each Test will be of 25 Marks.
Each Test Syllabus Weightage: Range should be 20% - 30%**

| Group (Theory or Practical) | Group (Theory or Practical) Credit | Total Subject Credit | Category | % Weightage | Marks Weightage | |
|-----------------------------|------------------------------------|----------------------|-------------------------------------|----------------------------|-----------------|------------|
| Theory | 5 | 5 | MCQ | 45% | 45 | |
| Theory | | | Theory Descriptive | 15% | 15 | |
| Theory | | | Formulas and Derivation | 0% | 0 | |
| Theory | | | Numerical | 40% | 40 | |
| Expected Theory % | 100% | | | Calculated Theory % | 100% | 100 |
| Practical | 0 | | Individual Project | 0% | 0 | |
| Practical | | | Group Project | 0% | 0 | |
| Practical | | | Internal Practical Evaluation (IPE) | 0% | 0 | |
| Practical | | | Viva | 0% | 0 | |
| Practical | | | Seminar | 0% | 0 | |
| Expected Practical % | 0% | | Calculated Practical % | 00% | 00 | |
| Overall % | 100% | | | 100% | 100 | |

Course Outcome

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| 1 | Understand the basic structure and gain knowledge about various functional units of digital computer. |
| 2 | Understand the instruction cycle, assembler unit and apply the set of instructions for creating assembly language programs. |
| 3 | Analyze instruction operations and evaluate the processor performance using parallel processing. |
| 4 | Analyze the organization of memory and understand the basics of I/O. |

Suggested Reference Books

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|---|---|
| 1 | M. Morris Mano, Computer System Architecture, Pearson |
| 2 | M. Morris Mano, Digital Logic and Computer Design, PHI |
| 3 | Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, Sixth Edition, PHI |
| 4 | M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY |
| 5 | John Hayes, Computer Architecture and Organization, McGrawHill |

List of Open Source Software/Learning website

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|---|---|
| 1 | https://onlinecourses.nptel.ac.in/noc21_cs61/preview |
| 2 | web.stanford.edu/class/ee282/ |