LOK JAGRUTI UNIVERSITY (LJU)

INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Information Technology (702)

Bachelor of Technology (B.E.) – Semester – III

Course Code:	**017023391**
Course Name:	**Digital Electronics**
Category of Course:	Professional Core Course (PCC)
Prerequisite Course:	--

Teaching Scheme				
Lecture (L)	**Tutorial (T)**	**Practical (P)**	**Credit**	**Total Hours**
4	**0**	**2**	**5**	**40**

Syllabus

Unit No.	Topic	Prerequisite Topic	Successive Topic	Teaching Hours
01	**Introduction to Digital Systems**			**3 (7%)**
	1.1 Digital Computers and Digital Systems: Definition and Basic Concepts	---	---	
	1.2 Number System: Decimal, Binary, Octal, Hexadecimal Numbers			
	1.3 Number System Conversion: Decimal to Binary, Decimal to Octal, Decimal to Hexadecimal, Binary to Decimal, Binary to Octal, Binary to Hexadecimal, Octal to Decimal, Octal to Binary, Octal to Hexadecimal, Hexadecimal to Decimal, Hexadecimal to Binary, Hexadecimal to Octal Conversions	Number System (017023391-Unit-1.2)		
02	**Binary Operations and Binary Codes**			**4 (10%)**
	2.1 Binary Arithmetic Operations: Addition, Subtractions, Decimal and Binary Complements, Subtraction using Decimal and Binary Complements	Binary Numbers (017023391-Unit-1.2)	Arithmetic and Logical Microoperations (017023401-Unit-2.3), Computer Arithmetic 017023401-Unit-8)	
	2.2 Binary Logical Operations: Logic Gates (NOT, AND, OR, NAND, NOR, EX-OR, EX-NOR), Universal Gates: NAND and NOR as NOT, AND, OR, Ex-OR, EX-NOR Gate			
	2.3 Binary Codes: Weighted Code (BCD,2421,84-2-1), Non-weighted Code (Excess-3, Gray), Error Detecting code: Parity Bit		---	
03	**Boolean Algebra and Boolean Functions**			**3 (6%)**
	3.1 Basic Theorems and Properties of Boolean Algebra	Binary Logical Operations (017023391-Unit-2.2)	---	
	3.2 Boolean Function: Formation of Logical Expression and Logic Diagram			
	3.3 Simplification of Boolean Function using Basic theorems	Boolean Function (017023391-Unit-3.1)		
04	**Boolean Function Minimizations**			**5 (14%)**
	4.1 Representation of Boolean Function: Canonical Form and Standard Form	Basic Theorems and Properties of Boolean Algebra (017023391-Unit- 3.1), Boolean Function (017023391-Unit-3.2)	---	
	4.2 Simplification using Karnaugh Map: 2 variable, 3 variable, 4 variable K-Map for SOP and POS Simplification, Don't care Condition			
	4.3 NAND and NOR Implementation			
	4.4 Tabulation Method (Quine-McCluskey method)			
05	**Combinational Logic Circuits-I**			**4 (10%)**
	5.1 Introduction of Combinational logic circuit	---	---	
	5.2 Adders: Block diagram, Truth Table, Logical Equation and Logic Diagram of Half Adder and Full Adder	Binary Arithmetic Operations (017023391-Unit-2.1)	Arithmetic Micro-operations (017023401-Unit-2.3), Arithmetic Logical Shift Unit (017023401-Unit-2.4)	
	5.3 Subtractors: Block diagram, Truth Table, Logical Equation and Logic Diagram of Half Subtractor and Full Subtractor			
	5.4 Binary Serial and Parallel Adder: Logic diagram and Working Principle			
	5.5 BCD Adder: Logic Diagram and Working Principle	Binary Adders (017023391-Unit-5.3)		
06	**Combinational Logic Circuits-II**			**5 (13%)**
	6.1 Multiplexers: 2 x 1 MUX, 4 x 1 MUX, 8 x 1 MUX, Example on Design of Multiplexer, Function Implementation using MUX	Binary Logical Operations (017023391-Unit-2.2)	Bus and Memory Transfer (017023401-Unit-2.2)	
	6.2 De-multiplexers: 1 x 2 De-MUX, 1 x 4 De-MUX, 1 x 8 De-MUX			
	6.3 Decoder: 2 x 4 and 3 x 8 Decoder, Example on Design of Decoder, Function Implementation using Decoder			
	6.4 Encoder: 4 x 2 and 8 x 3 Encoder			
	6.5 Code Converter: Binary to Gray, Gray to Binary Code, BCD to Seven Segment code converter	Binary Code (017023391-Unit-2.3), Logic Gates (017023391-Unit-2.2)	---	
	6.6 Comparator: 1- Bit Comparator, 2- Bit Comparator, 4- Bit Comparator			
	6.7 Parity Generator: Implementation of 3-bit Even and Odd Parity Generator			
	6.8 Parity Checker: Implementation of 4-bit Even and Odd Parity Checker			
07	**Sequential Logic Circuits – I**			**5 (13%)**
	7.1 Introduction to Sequential logic circuit	---	---	
	7.2 Latch: SR Latch, Difference between Latch and Flip-Flop	Logic Gates (017023391-Unit-2.2)	---	
	7.3 Flip-Flops: SR, JK, T and D Flip-Flop (Block Diagram, Logic Diagram, Truth Table and Excitation table)			
	7.4 Triggering of Flip-Flops: Positive and Negative Edge Triggered SR, JK, T and D Flipflop (Block Diagram, Logic Diagram, Truth Table and Waveforms)	Flip-Flops (017023391-Unit-7.2)		
	7.5 Race around condition and Master-Slave JK Flip-Flop			

	7.6 Conversion of Flip-Flops			
08	**Sequential Logic Circuits – II**			
	8.1 Register and Shift Registers: Classification of Shift Register, Logic Diagram and Working principle of Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out, Parallel In Parallel Out, Bidirectional and Universal Shift Register	Flip-Flops (017023391-Unit-7.2)	---	**4 (12%)**
	8.2 Counters: Logic Diagram, Working principle and Waveforms of Asynchronous Up, Asynchronous Down, Asynchronous Up/Down, Synchronous Up, Synchronous Down, Synchronous Up/Down Counters and Modulo Counters: Example on Design of Asynchronous and Synchronous Counter			
	8.3 Shift Register Counter: Logic Diagram, Working principle and Waveforms of Ring and Johnson Counter			
09	**Programmable Logic Device**			
	9.1 ROM: Classification of ROM (MROM, PROM, EPROM, EEPROM), ROM as PLD: Basic Concept, Logic Diagram and Examples of Function Implementation using ROM	Logic Gates (017023391-Unit-2.2)	Main Memory (017023401-Unit-9.1)	**4 (10%)**
	9.2 PAL: Basic Concept, Logic Diagram and Examples of Function Implementation using PAL		---	
	9.3 PLA: Basic Concept, Logic Diagram and Examples of Function Implementation using PLA			
	9.4 FPGA: Block Diagram, Working and Advantage of FPGA	PLA (017023391-Unit-9.3)		
10	**Digital Logic Families**			
	10.1 Classification of Logic Families	Logic Gates (017023391-Unit-2.2)	---	**3 (5%)**
	10.2 Characteristics of Logic Families: Fan-in, Fan-Out, Power-Dissipation, Noise Margin and Propagation Delay			
	10.2 Comparison of Logic Families: TTL and CMOS			
	10.3 Two input NAND gate using TTL: Circuit Diagram and Working Principle			
	10.4 NOT, NAND and NOR gate using CMOS Logic: Circuit Diagram and Working Principle			

Sr No.	Practical Title	Link to Theory Syllabus
1	Implementation of Basic logic gates and verify its truth-tables.	Unit-2
2	Verify the NAND and NOR gates as universal logic gates.	Unit-2
3	Design and verification of the truth tables of Half and Full adder circuits.	Unit-5
4	Design and verification of the truth tables of Half and Full subtractor circuits.	Unit-5
5	Design and implementation of 4:1 Multiplexer using logic gates	Unit-6
6	Design and implement 3:8 Decoder using logic gates	Unit-6
7	Design and verify the truth tables of different flip-flops	Unit-7
8	Design various 4-bit shift registers using flip flops	Unit-8
9	Design of ripple up and down counters and modulo-N counter using flip-flops	Unit-8
10	Design of synchronous up and down counter using flip-flops	Unit-8

Major Components/ Equipment	
Sr. No.	**Component/Equipment**
1	Computer Systems
2	NI Multisim/ Logisim /CEDAR Logic Simulator

Proposed Theory + Practical Evaluation Scheme by Academicians (% Weightage Category Wise and it's Marks Distribution)					
L :	**4**	**T:**	**0**	**P:**	**2**
Note : In Theory Group, Total 4 Test (T1+T2+T3+T4) will be conducted for each subject. Each Test will be of 25 Marks. Each Test Syllabus Weightage: Range should be 20% - 30%					
Group (Theory or Practical)	**Group (Theory or Practical) Credit**	**Total Subject Credit**	**Category**	**% Weightage**	**Marks Weightage**
Theory	**4**	**5**	MCQ	28%	35
Theory			Theory Descriptive (Mainly Programming)	4%	5
Theory			Formulas and Derivation	0%	0
Theory			Numerical	48%	60
Expected Theory %	**80%**		**Calculated Theory %**	**80%**	**100**
Practical	**1**		Individual Project	0%	0
Practical			Group Project	10%	50
Practical			Internal Practical Evaluation (IPE)	10%	50
Practical			Viva	0%	0
Practical			Seminar	0%	0
Expected Practical %	**20%**		**Calculated Practical %**	**20%**	**100**
Overall %	**100%**			**100%**	**200**

Course Outcome	
1	To gain knowledge about basic concepts of digital system including number system, binary codes and boolean theorems.
2	Apply boolean mapping methods to simplify boolean functions and design basic combinational circuits.
3	Design and analyze various combinational logic circuits and basic sequential logic circuits and verify its functionalities.
4	Design and analyze various digital circuits using sequential logic, PLDs and compare basic logic families.
Suggested Reference Books	
1	Digital logic and computer design, M Morris Mano, Pearson Education
2	Fundamentals of Digital Circuits, A. Anand kumar, Prentice Hall India
3	Digital Principles and Applications, Malvino and Leach, McGraw-Hill Education
4	Digital Logic Design, Holdsworth, Elsevier Science
5	Digital Fundamentals, Thomas L Floyd, Pearson Education

List of Open Source Software/Learning website	
1	www.nptel.ac.in
2	https://de-iitr.vlabs.ac.in/Introduction.html
3	Software- NI Multisim Simulator

Practical Project/Hands on Project		
Sr. No.	**Project List**	**Linked with Unit**
1	Design and Implementation of Decimal to binary converter. **Equipment's/Tools:** Diodes, Push buttons & LEDs	Unit 2
2	Design and Implement of Parking light mechanism. **Equipment's/Tools:** Logic Gate ICs, PCB & LEDs	Unit 2
3	Design and Implement Adder-Subtractor circuit using logic gates. **Equipment's/Tools:** Logic Gate ICs, PCB & LEDs	Unit 5
4	Design and Implement multiplexers and demultiplexers. **Equipment's/Tools:** ICs, PCB & LEDs	Unit 5
5	Design and Implement various Flip-flops using universal gates ICs. **Equipment's/Tools:** Logic Gate ICs, PCB & LEDs	Unit 7
6	Design and Implement various counters and shift register circuits. **Equipment's/Tools:** Counters, ICs, PCB & LEDs	Unit 8
7	Design and Implementation 7-segment counter. **Equipment's/Tools:** Logic/Counter ICs, PCB & 7 Segment Display	Unit 8
8	Design and Implement Digital object counter. **Equipment's/Tools:** Logic/Counter ICs, PCB & 7 Segment Display	Unit 8
9	Design and Implement Logic gates using TTL circuit. **Equipment's/Tools:** Transistors, PCB & LEDs	Unit 10
10	Design and Implementation of Water level indicator circuit.	Unit 10

	Equipment's/Tools: Transistors, PCB & LEDs	