LOK JAGRUTI UNIVERSITY (LJU)

INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication (707)

Bachelor of Engineering (B.E.) – Semester – II

Course Code:	**017073202**
Course Name:	**Digital circuits and Logic Design**
Category of Course:	Professional Core Course (PCC)
Prerequisite Course:	--

Teaching Scheme				
Lecture (L)	**Tutorial (T)**	**Practical (P)**	**Credit**	**Total Hours**
5	**0**	**2**	**6**	**50**

Syllabus

Unit No.	Topic	Prerequisite Topic	Successive Topic	Teaching Hours
01	**Introduction to Digital Systems, Number Systems and Codes**			**4 (8%)**
	1.1 Introduction to Digital electronics	---	---	
	1.2 Binary Digits, Logic Levels, and Digital Waveforms	---	---	
	1.3 Introduction to Number Systems-Types-Decimal, Binary, Octal, Hexadecimal; Conversion from one number system to other(Decimal, Binary, Octal, Hexadecimal), BCD code	---	---	
	1.4 Digital Codes -Excess-3 code, Gray code, Binary to Excess -3 code conversion and vice versa.	---	---	
02	**Logic Gates**			**5 (10%)**
	2.1 Logical Operators, Boolean Algebra	Introduction to Number Systems (017073202 – Unit-1.3)	---	
	2.2 Logic Gates	Logic Levels (017073202 – Unit-1.2)	Universal Gates (017073403 – Unit-1.2)	
	2.3 Universal Gates and realization of other gates using universal gates	Logic Gates (017073202 – Unit-2.2)	---	
03	**Boolean Algebra and Simplification**			**5 (10%)**
	3.1 Understanding POS and SOP expressions for 2 to 4 variables: Min-term and Max-term	---	---	
	3.2 K-map minimization and implementation of Boolean function using Logic gates (4 Literals)	Logic Gates (017073202 – Unit-2.2)	---	
	3.3 Quine- McCluskey methods for optimization (Tabulation Method)	Understanding POS and SOP expressions for 2 to 5 variables: Min-term and Max-term (017073202 – Unit-3.1)	---	
04	**Combinational Logic Circuits**			**6 (12%)**
	4.1 Basics of Combinational logic design: 1. Half Adder and Full Adder 2. Half Subtractor and Full Subtractor	Boolean Algebra (017073202 – Unit-2.1)	Half Adder and Full Adder (017073403 – Unit-3.1) CMOS Logic circuits (017073502 – Unit-8.2)	
	4.2 Code Converters: 1. Binary to Gray Conversion using combination circuit 2. Binary to Excess 3 conversion using combination circuit	Adder (017073202 – Unit-4.1)		
	4.3 Parity bit Generators/Checkers, (3 bits) Magnitude Comparator (2 bits)	---	---	
	4.4 Multiplexers (types 2x1, 4x1 and 8x1) and Decoders (Types 2x4, 3x8)	---	Types of Mux (017073403 – Unit-4.1) Types of DeMux (017073403 – Unit-4.2)	
05	**Sequential Circuits**			**6 (12%)**
	5.1 Concept of sequential circuit using significance of clock signal	Logic Gates (017073202 – Unit-2.2)		
	5.2 SR Flip-flop, D Flip-flop, JK Flip-flop, T Flip-flop	Logic Gates (017073202– Unit-2.2)	Types of Flip flop (017073403 – Unit-6.1) The SR Latch Circuit (017073502 – Unit-9.2) CMOS D-Latch and Edge-Triggered Flip-flop (017073502 – Unit-9.4)	
	5.3 Master-slave JK Flip-flop	---	---	
06	**Counter and Shift Register**			**5 (10%)**
	6.1 Synchronous and Asynchronous counter	SR Flip-flop, D Flip-flop, JK Flip-flop, T Flip-flop (017073202 – Unit-5.2)	---	
	6.2 Up Counter(4-bit) and Down Counter (4-bit)	SR Flip-flop, D Flip-flop, JK Flip-flop, T Flip-flop (017073202 – Unit-5.2)	---	
	6.3 Shift registers (4-bit)	SR Flip-flop, D Flip-flop, JK Flip-flop, T Flip-flop (017073202 – Unit-5.2)	---	

07	**Synchronous Finite State Machine**			**5 (10%)**
	7.1 Design and analysis of synchronous sequential circuits: Basic Concepts of state diagram, state tables and state machines	Synchronous and Asynchronous counter (017073202 – Unit-6.1)	---	
	7.2 Design of Melay and Moore based FSM using D-Flip Flop	Synchronous and Asynchronous counter (017073202 – Unit-6.1)	Mealy Based FSM (017073403 – Unit-8.1) Moore Based FSM (017073403 – Unit-8.2)	
08	**Asynchronous Finite State Machine**			**5 (10%)**
	8.1 Design and Analysis of asynchronous sequential circuits	Synchronous and Asynchronous counter (017073202 – Unit-6.1)	---	
	8.2 Design issues in asynchronous FSM.	---	---	
09	**Programmable Logic Devices**			**5 (10%)**
	9.1 Introduction to Programmable Logic Devices	Logic Gates (017073202– Unit-2.2)	---	
	9.2 Programmable Logic Arrays (PLA)	Introduction to Programmable Logic Devices (017073202 – Unit-9.1)	---	
	9.3 Programmable Array Logic (PAL)	---	---	
10	**Logic Families**			**4 (8%)**
	10.1 Building Basic Logic Gates with Diodes	---	---	
	10.2 Digital Logic Families: RTL, DTL, TTL, CMOS	---	---	

Sr No.	Practical Title	Link to Theory Syllabus
1	Realize practically and verify truth table of logic gates: AND, OR, NOT, NAND, NOR, XOR and XNOR.	Unit-2
2	Design AND, OR, NOT using universal gates (NAND and NOR) and also verify truth tables.	Unit-2
3	Verify Boolean Laws using truth table and reduce the given Boolean function: XYZ	Unit-2
4	Design Code Convertors: 1. Binary to Gray Generator 2. Gary to Binary Generator	Unit-1,2
5	Design Adders and Subtractors: 1. Half Adder and Full Adder 2. Half Subtractor and Full Subtractor	Unit-3,4
6	Design BCD to Seven Segment Display and release the conversion on digital trainer board	Unit-3,4
7	Design 4:1 Multiplexer using following logic gates: 1. AND, OR, NOT 2. NAND	Unit-4
8	Design 1:4 Demultiplexer using following logic gates: 1. AND, OR, NOT 2. NAND	Unit-4
9	Design 2-bit encoder and decoder using logic gates.	Unit-4
10	Design 2-bit and 4-bit Magnitude Comparator	Unit-4
11	Verify the truth tables of 1. RS Flip Flop 2. D Flip Flop 3. JK Flip Flop 4. T Flip Flop	Unit-5
12	Design and implement 3-bit up and down counters	Unit-6
13	Design and implement 4-bit shift (LEFT-RIGHT) registers	Unit-7

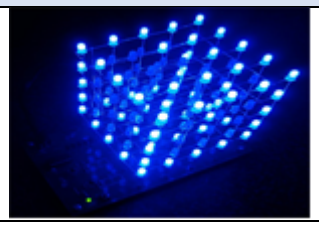
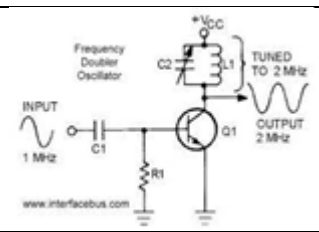
Major Components/ Equipment

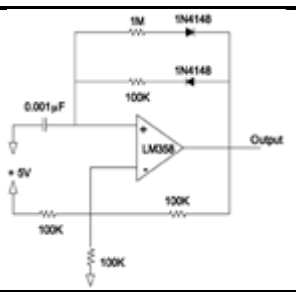
Sr. No.	Component/Equipment
1.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
2.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
3.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
4.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
5.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
6.	Digital Circuit Trainer Kit (Logic gates ICs, In-built Clock, Seven Segment Display), Connecting Wires, Bread-Board, DC Power Supply, LEDs
7.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
8.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
9.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
10.	Digital Circuit Trainer Kit (Logic gates ICs and in-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
11.	Digital Circuit Trainer Kit (Logic gates and Flip-Flop ICs, In-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
12.	Digital Circuit Trainer Kit (Logic gates and Counter-Register ICs, In-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs
13.	Digital Circuit Trainer Kit (Logic gates and Counter-Register ICs, In-built Clock), Connecting Wires, Bread-Board, DC Power Supply, LEDs

Proposed Theory + Practical Evaluation Scheme by Academicians (% Weightage Category Wise and it's Marks Distribution)					
L :	**5**	**T:**	**0**	**P:**	**2**
Note : In Theory Group, Total 4 Test (T1+T2+T3+T4) will be conducted for each subject. Each Test will be of 25 Marks. Each Test Syllabus Weightage: Range should be 20% - 30%					
Group (Theory or Practical)	**Group (Theory or Practical) Credit**	**Total Subject Credit**	**Category**	**% Weightage**	**Marks Weightage**
Theory	**5**	**6**	MCQ	50%	60
Theory			Theory Descriptive	12%	15
Theory			Formulas and Derivation	0%	0
Theory			Numerical	21%	25
Expected Theory %	**83%**		**Calculated Theory %**	**83%**	**100**
Practical	**1**		Individual Project	0%	0
Practical			Group Project	5%	30
Practical			Internal Practical Evaluation (IPE)	12%	70
Practical			Viva	0%	0
Practical			Seminar	0%	0
Expected Practical %	**17%**		**Calculated Practical %**	**17%**	**100**
Overall %	**100%**			**100%**	**200**

Course Outcome	
	Upon completion of the course students will be able to
CO1	Students will get familiar with digital Integrated circuit of digital logic families.
CO2	Learn the basic concepts of digital circuits and system which leads to design of complex digital system such as microprocessor.
CO3	Learn the combinational and sequential circuit which help them to understand data storage in memory different binary operations in CPU.
CO4	Learn strong foundation in the core fundamentals of digital technology using VLSI by plentiful illustrations and application."
Suggested Reference Books	
1	Morris Mano, "Digital Design", Prentice Hall of India.
2	Digital Principles and Applications By Malvino & Leach, Seventh Edition, McGraw-Hill Education
3	Digital Design M. Morris Mano and Michael D. Ciletti, Pearson Education
4	Digital Principles and Applications By Malvino & Leach, Seventh Edition, McGraw-Hill Education
5	Digital Electronics: Principles and Integrated Circuits By A.K. Maini, Wiley India Publications
6	Anand Kumar, "Switching Theory and Logic Design", Prentice Hail of India

List of Open Source Software/Learning website	
1	https://www.circuitlab.com
2	http://vlabs.iitb.ac.in
3	https://www.iitg.ac.in

Practical Project/Hands on Project		
Sr. No.	**Project List**	**Linked with Unit**
1	5 X 5 X 5 LED cube generating different 3D patterns by multiplexing. 	All Units
2	Simple ALU.	All Units
3	Design of Frequency Multiplier. 	All Units

4	A pulse generator/monitor circuit. 	All Units
5	Error detection Circuit for communication systems.	All Units