



**Lok Jagruti Kendra University**  
University with a Difference

# **Diploma in Electronics & Communication Engineering**



**Course Code: 025030503  
VLSI Technology**

<b>Programme / Branch Name</b>		Diploma in Electronics & Communication Engineering				
<b>Course Name</b>	VLSI Technology				<b>Course Code</b>	025030503
<b>Course Type</b>	HSSC	BSC	ESC	PCC	OEC	PEC

**Legends:** HSSC: Humanities and Social Sciences Courses  
ESC: Engineering Science Courses  
OEC: Open Elective Courses

BSC: Basic Science Courses  
PCC: Program Core Courses  
PEC: Program Elective Courses

## 1. Teaching and Evaluation Scheme

Teaching Hours / Week / Credits				Evaluation Scheme			
L	T	P	Total Credit	CCE	SEE (Th)	SEE (Pr)	Total
4	0	2	5	50	50	50	100

**Legends:**

L: Lectures T: Tutorial P: Practical  
CCE: Continuous & Comprehensive Evaluation  
SEE (Th): Semester End Evaluation (Theory)  
SEE (Pr): Semester End Evaluation (Practical)

## 2. Prerequisite

- ✓ Basics of Digital Electronics
- ✓ Basics of Transistors
- ✓ Inverter Circuit
- ✓ Combinational Logic Circuit
- ✓ Sequential Logic Circuit

## 3. Rationale

In the study of this course, the students will understand and learn the basic skills to develop codes for VLSI circuits through VHDL programming. VLSI Design is a core subject for the knowledge of which is essential for electronics and communication engineering diploma holders and they need to assimilate it to succeed in the electronic industry. Very large-scale integration is the process of making a microcircuit by combining many MOS transistors onto one chip. It is a microcircuit chips widely adopted, enabling complex semiconductor and telecommunication technologies to be developed. In laboratory part of this course, students will be given exposure to hardware description language such as VHDL for automated design of digital circuits. This subject is very important for the students who will be in future would like to pursue their career in VLSI domain.

## 4. Objectives

- ✓ Learn about VLSI technology.
- ✓ Gain a greater understanding of the advantages of VLSI technology.
- ✓ Learn how VLSI technology is used in today's devices and systems.
- ✓ Develop VHDL Programs related to Combinational circuits
- ✓ Develop VHDL Programs related to Sequential circuits



## 5. Contents

Unit No.	Unit Name	Topics	Learning Outcome	% Weightage	Hours
1	<b>Introduction to VLSI Design</b>	1.1. Overview of VLSI design Methodologies 1.2. VLSI Design Flow 1.3. Design Hierarchy 1.4. Concepts of Regularity, Modularity, and locality 1.5. VLSI Design Styles 1.6. Design Quality	<ul style="list-style-type: none"> <li>• Definition, History and Overview of VLSI</li> <li>• The Y Chart</li> <li>• Concepts of Regularity, Modularity and Locality</li> <li>• FPGA</li> <li>• Gate Array Design</li> <li>• Standard Cell Based Design</li> <li>• Full Custom Design</li> <li>• Testability</li> <li>• Yield and Manufacturability</li> <li>• Reliability</li> <li>• Technology Updateability</li> </ul>	10	10
2	<b>MOS Transistor</b>	2.1 The MOS structure 2.2 The MOS system under external bias 2.3 Structure and MOSFET transistor 2.4 The Threshold Voltage 2.5 Operation of MOSFET Transistor 2.6 Characteristics of MOSFET 2.7 Small Geometry Effects 2.8 MOSFET Capacitance	<ul style="list-style-type: none"> <li>• Basics of MOSFET</li> <li>• MOS Structure</li> <li>• Energy Band Diagram of MOS</li> <li>• Circuit Symbol</li> <li>• Gradual Channel Approximation</li> <li>• Channel Length Modulation</li> <li>• Substrate Bias Effect</li> <li>• Short Channel Effects</li> <li>• Narrow Channel Effects</li> <li>• Limitation Imposed by Small-Device Geometry</li> <li>• Oxide-Related Capacitance</li> <li>• Junction Capacitance</li> </ul>	20	10

3	<b>MOS Inverters</b>	3.1 Introduction to Inverter 3.2 Resistive Load Inverter 3.3 Inverter with n-type MOSFET Load 3.4 CMOS Inverter 3.5 Cascade CMOS Inverter Stages 3.6 Delay Time Definition 3.7 Switching Power Dissipation of CMOS Inverter	<ul style="list-style-type: none"> <li>• Voltage Transfer Characteristics (VTC)</li> <li>• Noise Immunity and Noise Margin</li> <li>• Power Consumption and Chip Area</li> <li>• Enhancement Load nMOS Inverter</li> <li>• Depletion Load nMOS Inverter</li> <li>• Power Consumption and Chip Area</li> <li>• Circuit Diagram and Operation</li> <li>• Circuit Analysis</li> <li>• Operation Modes</li> <li>• Operation Regions</li> <li>• Propagation Time Delay</li> <li>• Derivation of Delay Expression</li> <li>• Rise Time and Fall Time</li> <li>• Power Dissipation</li> </ul>	20	10
4	<b>Combinational &amp; Sequential MOS Logic Circuits</b>	4.1 Basics of Combinational Circuit 4.2 Two Input NOR Gate with Depletion nMOS Load 4.3 Two Input NAND Gate with Depletion nMOS Load 4.4 Two Input NOR Gate with CMOS 4.5 Two Input NAND Gate with CMOS 4.6 Complex Logic Circuit 4.7 Sequential MOS Logic Circuits 4.8 NOR Based SR Latch Circuit 4.9 NAND Based SR Latch Circuit 4.10 Clocked NOR-Based SR Latch Circuit	<ul style="list-style-type: none"> <li>• Logic Symbol, Truth Table and Circuit Diagram of NOR Gate</li> <li>• Generalized NOR Structure with Multiple Inputs</li> <li>• Logic Symbol, Truth Table and Circuit Diagram of NAND Gate</li> <li>• Generalized NAND Structure with Multiple Inputs</li> <li>• Circuit Diagram &amp; Equivalent Circuit of NOR and NAND Gate with CMOS</li> <li>• Realization using nMOS and CMOS of Logic Circuit</li> <li>• Block Diagram &amp; Classification of Sequential Circuit</li> <li>• Symbol, Logic Diagram, Circuit Diagram and Truth Table of SR Latches</li> </ul>	30	16

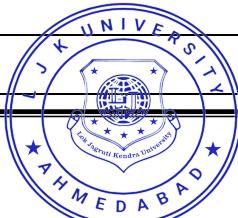
5	<b>Introduction to VHDL</b>	5.1 Introduction to VHDL Language	<ul style="list-style-type: none"> <li>• VHDL Language Capabilities</li> <li>• Hardware Abstraction</li> <li>• Design Unit of VHDL</li> <li>• Logical and Relational Operations</li> <li>• Shift and Rotate Operations</li> <li>• Adding and Multiplying Operators</li> <li>• Miscellaneous Operators</li> <li>• Design OR, AND, NOT, NOR, NAND XOR and XNOR Logic Using VHDL Code</li> <li>• Design Half and Full Adder Using VHDL Code</li> <li>• Design Half and Full Subtractor Using VHDL Code</li> <li>• Design 4:1 MUX and 1:4 DEMUX Using VHDL Code</li> <li>• Design 4:2 Encoder and 2:4 Decoder Using VHDL Code</li> <li>• Design SR, JK, D and T Flip-Flop Using VHDL Code</li> </ul>	20	10
		5.2 Fundamental Operators			
		5.3 Design of Logic Gates Using VHDL Code			
		5.4 Design of Arithmetic Logic Circuits Using VHDL Code			
		5.5 Design of Combinational Logic Circuits Using VHDL Code			
		5.6 Design of Sequential Logic Circuits Using VHDL Code			

**Total Hours** **56**

## 6. List of Practical's / Exercises

The practical/exercises should be properly designed and implemented in an attempt to develop different types of skills that students can acquire the competencies/programme outcomes. Following is the list of practical exercises for guidance.

Sr. No	Practical / Exercises	Key Competency	Hours
1	Introduction to VHDL	Introduction	2
2	To study VHDL entities and coding styles	Simulation	2
3	To study signals and data types.	Simulation	2
4	To implement various basic logic gates using VHDL.	Simulation	2
5	To implement universal logic gates using VHDL.	Simulation	2
6	To implement different Flip-Flop using VHDL.	Simulation	2
7	To implement Multiplexer using VHDL.	Simulation	2
8	To implement Demultiplexer using VHDL.	Simulation	2
9	To implement Half adder using VHDL.	Simulation	2



10	To implement Full adder using VHDL.	Simulation	2
11	To implement Half subtractor using VHDL.	Simulation	2
12	To implement Full subtractor using VHDL.	Simulation	2
13	To implement counter using VHDL	Simulation	2
14	To implement decoder using VHDL.	Simulation	2
15	To implement encoder using VHDL.	Simulation	2
16	To implement SR flip flop using VHDL.	Simulation	2
17	To implement JK flip flop using VHDL.	Simulation	2
18	To implement D flip flop using VHDL.	Simulation	2
19	To implement T flip flop using VHDL.	Simulation	2

## 7. Suggested Specification for Evaluation Scheme

Unit No.	Unit Name	Distribution of Topics According to Bloom's Taxonomy					
		R %	U %	App %	C %	E %	An %
1	Introduction to VLSI Design	40	20	20	0	10	10
2	MOS Transistor	20	20	15	20	20	5
3	MOS Inverters	20	20	20	15	10	15
4	Combinational & Sequential MOS Logic Circuits	20	20	15	20	10	15
5	Introduction to VHDL	30	20	20	10	10	10

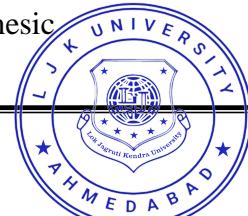
**Legends:** R-Remembering  
U- Understanding  
App- Applying  
C- Creating  
E- Evaluating  
An- Analyzing

## 8. Textbooks

- 1) CMOS Digital Integrated Circuits - Analysis and Design by Sung-Mo Kang, Yusuf Leblebici, TMH
- 2) VLSI DESIGN – Jagdeep Kaliraman, Praveen Kumar Gupta, Tejvir Singh Chhikara, Satya Prakashan
- 3) VLSI – Dr. R. K. Singh, S. K. Kataria & Sons

## 9. Reference Books

- 1) CMOS VLSI Design - Weste, Harris, Banerjee – Pearson
- 2) Principle of CMOS VLSI Design – A system Perspective by Neil D. E. Weste, Kamran Eshraghian TATA McGraw-Hill Pub. Company Ltd.
- 3) Basic VLSI Design by Pucknell and Eshraghian, PHI, 3rd edition.
- 4) Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
- 5) Introduction to VLSI Circuits & Systems – John P. Uyemura
- 6) Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic



## 10. Open Sources (Website, Video, Movie)

1. [https://www.tutorialspoint.com/vlsi\\_design/vlsi\\_design\\_digital\\_system.htm](https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm)
2. [http://ece-research.unm.edu/jimp/vlsi/slides/c1\\_intro.html](http://ece-research.unm.edu/jimp/vlsi/slides/c1_intro.html)
3. <https://www.geeksforgeeks.org/vlsi-design-cycle/>
4. <https://www.javatpoint.com/vhdl>
5. <https://www.engineersgarage.com/vhdl-tutorial-1-introduction-to-vhdl/>